

ABSTRACT OF THE DISCLOSURE

A memory cell having improved interconnect. Specifically, a dynamic random access memory (DRAM) based content addressable (CAM) memory cell is provided. The lower cell plate of the storage capacitor is implemented to provide an interconnect for the access transistor and the CAM portion of the memory cell. Conductive plugs are coupled to each of the transistors and coupled directly to the lower cell plate of the capacitor.